AMENDMENTS TO THE SPECIFICATION

In the Title

Please replace the title with the following -- METHOD OF FORMING TRANSISTOR HAVING INSULATING SPACERS ON GATE SIDEWALLS --

In the Specification

Please insert as the first paragraph of the specification:

-- The present application is a divisional of U.S. Patent Application Serial Number 10/247,027 filed September 19, 2002, currently pending. --

Please delete the paragraph numbered **[0039]** beginning on page 13 and insert the following in place thereof:

-- **[0039]** After forming the insulating spacers, extension regions may be formed in the substrate adjacent to the insulating spacers at block 430. Doped extension regions may be formed by an ion implantation process in which the insulating spacers are used to align the dopants introduced into the substrate. Next, a source and a drain are formed at block 440. This may include performing a thermal anneal to electrically activate the source/drain terminals, as well as the doped extension regions. The method for fabricating the transistor terminates at block 450 ~~360~~, although it will be appreciated that other conventional operations will often be performed, for example to form contacts to the terminals of the transistor. --

Please delete the paragraph numbered **[0060]** beginning on page 23 and insert the following in place thereof:

-- **[0060]** Accordingly, Figures 5A-5G show a method for fabricating a transistor containing insulating spacers formed on the sidewalls of the gate, according to embodiments of the invention. ~~These will not be discussed in order to avoid obscuring the concepts of the invention.~~ The fabricated transistor has a number of advantages. One advantage is that given appropriate control over the width of the insulating spacers, the formation of the extension regions, and thermally induced encroachment of the extension regions beneath the gate, the insulating spacers may help reduce the overlap of the extension regions with the gate. This may help reduce capacitance that slows the switching speed of the transistor and help reduce standby leakage current. Another advantage is that processing techniques to form notches in the gate, which are known to be problematic, may be avoided. Yet another advantage is a reduction in the gate width, as will be discussed below. --